

J. Goel, G. Oransky, S. Yuan, P. O'Sullivan and J. Burch

TRW

Advanced Microwave Technology Department
One Space Park
Redondo Beach, California 90278

ABSTRACT

A multistage GaAs FET power amplifier, employing cascaded balanced stages using state-of-the-art 1/4, 1/2, and 1 watt devices, has been developed. A linear gain of 30 dB with 1.25 watts output has been achieved over a 17.7 to 19.4 GHz frequency band. The development and performance of the amplifier and its components are discussed.

Introduction

Studies of the growth in communications traffic indicate that the frequency spectrum allocated to fixed service satellites at C- and Ku-band will reach saturation by the early 1990's. K-band, with uplink frequencies at 27.5 to 30.0 GHz and downlink frequencies at 17.7 to 20.2 GHz is the next higher frequency band allocated for this purpose. Current plans for the development of satellite systems to implement this band include the possibility of a NASA demonstration experiment in the mid-1980's. System studies have identified the use of multibeam antenna systems as a major factor in achieving minimum cost and efficient use of frequency and orbital resources. Such multibeam systems, however, require reliable, efficient, lightweight, solid state transmitters. This amplifier has been developed for the downlink of a 30/20 GHz communication system.

This paper reports on the development of a GaAs FET amplifier capable of output power greater than 1 watt over a bandwidth of 17.7 to 19.4 GHz with a linear gain of 30 dB. Assembly techniques and test results for the amplifier and its circuit components will be discussed.

Passive Components

The most common transmission mode above 18 GHz is waveguide; however, it is easier to design GaAs FET amplifiers using microstrip transmission line. Generally, waveguide-to-SMA and SMA-to-microstrip transitions are used to bridge from waveguide to microstrip. The problem is that commercial SMA-to-microstrip launchers have unacceptable losses above 18 GHz. A lower loss direct waveguide-to-microstrip transition, which can be accomplished using a quarter-wave ridge transformer has been employed. Two such transitions connected back to back by 0.5 inches of 50 ohm microstrip line measure 0.5 dB or less loss from 17 to 21 GHz.

To achieve high power levels over a broad frequency range, some form of power combining is required. There are several approaches for realizing a practical hybrid coupler compatible with microstrip transmission line. These approaches are based on the proximity coupling of two adjacent quarter-wavelength microstrip lines.^{5,6,7} A six-finger interdigital coupler on 0.015 inch quartz was developed at TRW to fill this need. The coupler design was chosen for its low VSWR and high isolation features. A low VSWR thin film tantalum nitride load resistor was included on the same coupler substrate. The coupler test data indicate an equal power split with less than 0.5 dB loss over the 17 to 21 GHz range. Figure 1 shows a diagram of the coupler design.

Power Amplifier

Two important design considerations for an amplifier used in a spaceborne system application are performance and mean-lifetime-failure. The GaAs FETs developed for this design (Raytheon 872) were designed for minimum thermal resistance, minimum parasitic source inductance, and maximum high-power, broadband gain. The 1-watt FET design is shown in Figure 2. The sources are connected to the ground via holes etched in the thinned substrate, which is approximately 0.002 to 0.003 inches thick. This reduces thermal resistance and the parasitic source inductance. These two FET properties play an important role in the amplifier design and performance; low thermal resistance can be directly related to a longer device MTBF and results in a longer amplifier lifetime. Similarly, the parasitic source inductance will seriously affect the FET RF performance, particularly the bandwidth. Typical operating device junction temperatures are 110°F, corresponding to a 5 x 10⁶ hour MTBF. The high power and broadband characteristics of the FETs are acquired through a combination of material and physical device parameters.

Assembly of a single amplifier stage begins with Au/Ge eutectic soldering of the FET onto a gold-plated, copper chip carrier. The chips are then wire-bonded to the RF lines of gate and drain substrate assemblies. The substrate is 0.015 inch quartz, which has been Au/Ge eutectic soldered to a gold plated INVAR shim. An INVAR shim is used since its thermal expansion coefficient closely matches that of quartz, and therefore minimize the stresses built up during soldering. Quartz was chosen because of its low dielectric constant, low tangential loss, and good surface finish.

Amplifier design followed after device S-parameters were measured in test fixtures which closely simulated the actual mounting arrangement in the amplifier. Data were obtained on each device type, 1/4, 1/2, and 1 watt FETs up to 18 GHz, using an Automated Network Analyzer. The S-parameter data were then extrapolated to 21 GHz and matching circuits were designed and optimized over the 17 to 21 GHz frequency band using computer aided design programs. Circuit designs generated for the gate and drain substrate assemblies included a biasing filter, blocking capacitors, and some tuning pads.

Devices were then assembled into fixtures to measure and optimize their individual gain, bandwidth, and output power. A waveguide measurement system and a scalar network analyzer were used for testing. The devices were connected to this system using the waveguide-to-microstrip transitions discussed earlier. To facilitate assembly and tuning, the waveguide transitions were connected to a length of microstrip line in a housing which prevented waveguide mode propagation below 30 GHz. The devices being tested were then

connected to these lines. This type of test fixture keeps RF radiation to a minimum and helps in tuning the assembled MIC amplifier. After taking the data on these tuned individual devices, the results were analyzed. Devices were then selected for combining and were then tested as directly cascaded device pairs. With this accomplished, device pairs were then chosen for integration into the power amplifier.

A schematic diagram of the power amplifier is shown in Figure 3. The power amplifier can be divided as shown into two identically configured submodules. The submodules differ only in the device types used. Submodule No. 1 uses only 1/4-watt devices, whereas, submodule No. 2 has 1/2 and 1-watt devices. Since the first stages of a submodule are gain stages, devices were chosen for these stages for best gain characteristics. Subsequent stages were selected to operate in a balanced configuration using the interdigitated couplers described earlier. Each submodule was assembled and tested prior to final assembly of the amplifier. The submodules were then assembled into the complete power amplifier as shown in Figures 3 and 4. Data obtained from tests on the overall amplifier are shown in Figures 5 and 6. Figure 5 demonstrates the 30 ± 0.5 dB gain over the 1.7 GHz bandwidth. The Pin vs. Pout characteristic shown in Figure 5 demonstrates the 1.25-watt output power at the 1 dB gain compression point. The measured noise figure is 8.4 dB.

Conclusion

The development and performance of a 1.25 watt GaAs FET power amplifier with a linear gain of 30 ± 0.5 dB of gain over a bandwidth of 1.7 GHz centered at 18.5 GHz has been demonstrated. Assembly techniques for the amplifier and its components have been described.

Acknowledgement

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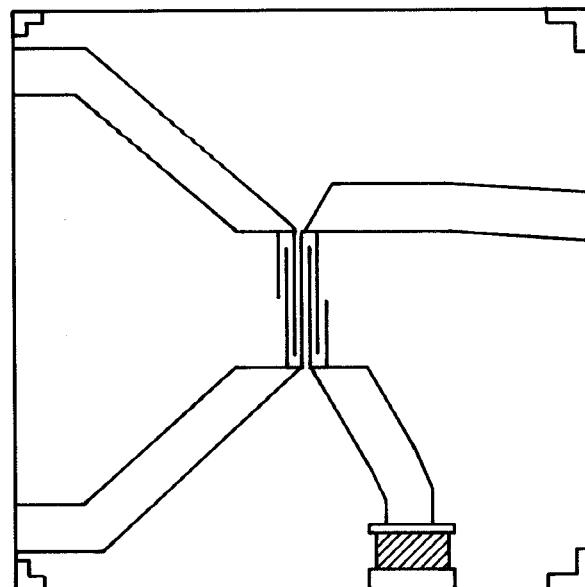


Figure 1. Six-Finger Interdigital Coupler Circuit Diagram

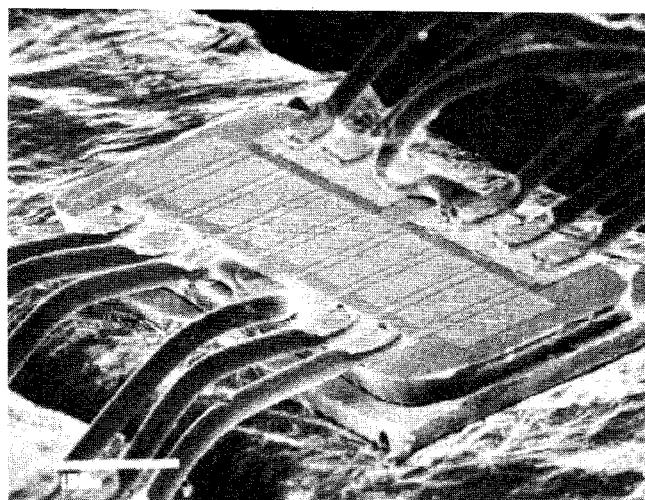


Figure 2. Raytheon 1-Watt GaAs FET

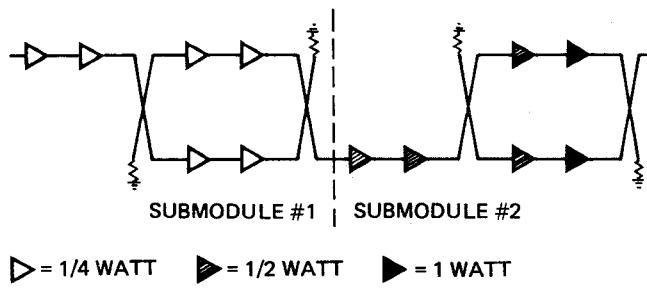


Figure 3. Schematic Diagram of the Power Amplifier

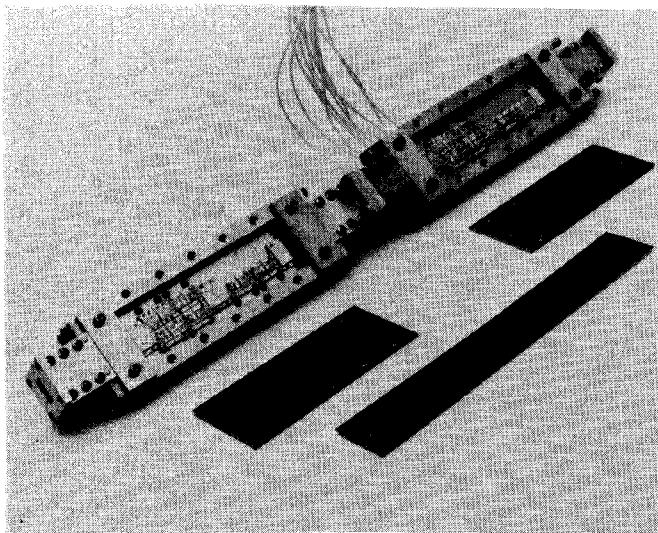


Figure 4. Picture of the Power Amplifier With Waveguide to Microstrip Transistions

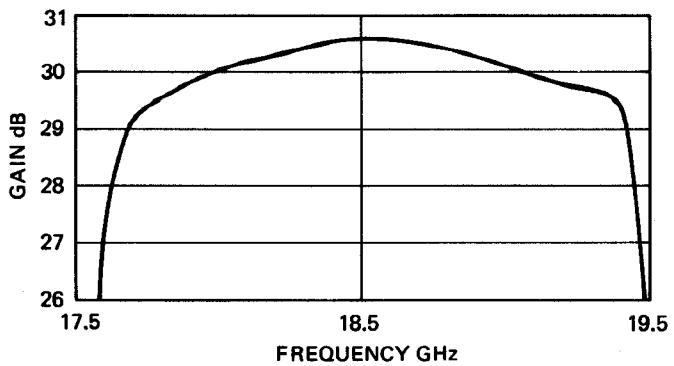


Figure 5. Frequency Response of the Power Amplifier at a 0 dBm Input Power Level

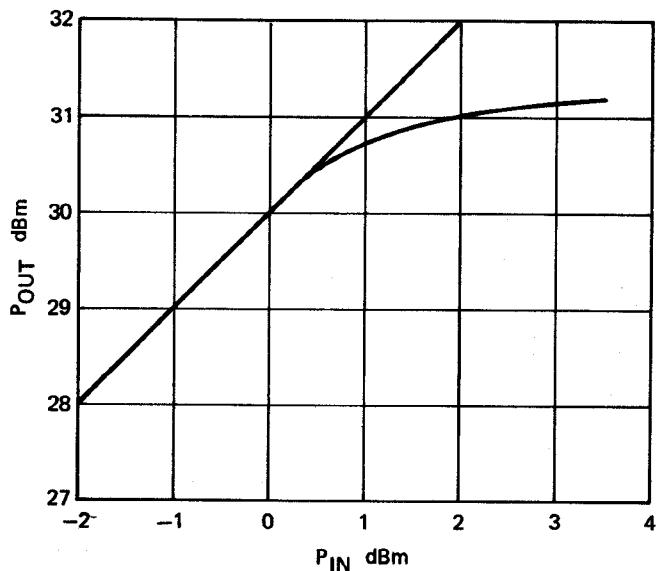


Figure 6. Pout vs. Pin for the Power Amplifier